Clock-Command Combined Carrier Coding (C5) – A DC Balanced Coding Scheme for Transmitting Messages with Clock

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Abstract:
A DC balanced coding scheme designed for transmitting messages along with clock in a single signal channel for digitization-at-detector applications is described in this paper. The primary feature of this scheme is that all the leading edges of the pulses represent correct clock time, while the message bits are encoded into the widths of the pulses. Therefore the pulse train can drive sequential logics directly just as an ordinary clock signal. Unlike other coding schemes, the one described here needs no channel initiation such as preamble, frame synchronization pattern, etc.

Summary:

In high-energy physics experiment detectors, it has become a trend to place the digitization devices close to the signal sources and to send digitized data via serial link to the data acquisition (DAQ) modules. The digitization devices usually need a clock signal derived by the data acquisition modules from a common timing reference. In addition to the clock, the DAQ system sometime sends various commands such as register loading, synchronization, trigger acceptance, etc. to the digitization devices. It is desirable and sometimes mandatory to transmit the clock and the messages through as few wires as possible.

There are high efficiency schemes to transmit clocks and messages through single channel, such as 8B/10B coding. However, relatively large amount of silicon resources are needed to recover the clock and data.

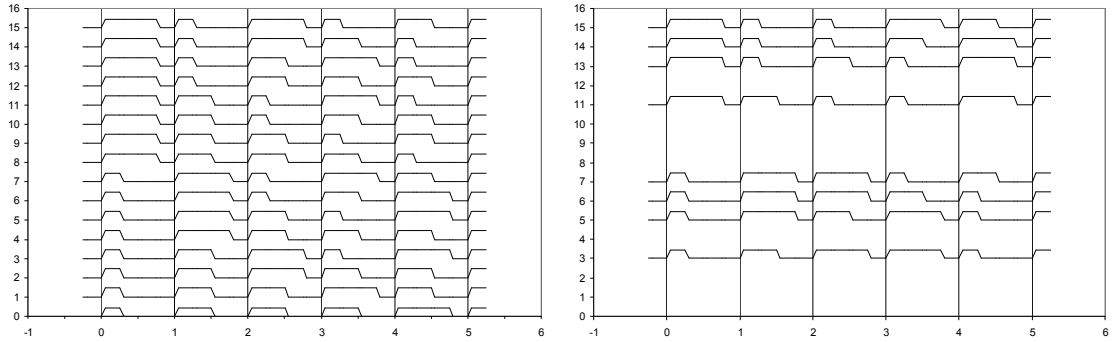
The digitization-at-detector application in HEP is at the other end of the spectrum. The amount of messages to be uploaded to the digitizer is not too large, so the channel efficiency needs not to be high. However, the FPGA for the digitizer can not be too big, so the clock and data recovery circuits must be very simple.

In this paper, we describe the "Clock-Command Combined Carrier Coding" (C5) scheme that is DC balanced and is designed to transmit clock the command messages together in a single channel (usually a pair of differential signals) with extremely simple clock and data recovery.

In the C5 scheme all the leading edges of all the pulses are at correct clock time, while the message bits are encoded into the widths of the pulses. Therefore practically there is no "recovery" needed for the clock. The pulse train can drive sequential logics directly just as an ordinary clock signal.

The C5 scheme is self-framed or self-synchronized; the channel initiation processes such as preamble, training pattern, frame synchronization pattern etc. are not needed. This will simplify the design of both the sender and the receiver.

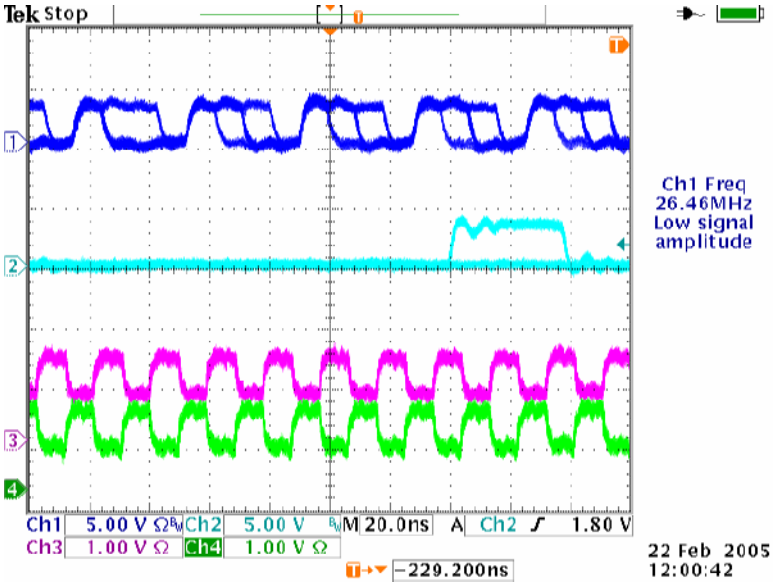
After a systematic selection, the 5-pulse trains as shown in the following pictures are employed in the C5 scheme. The pulse trains in the left and right pictures are assigned as data and control codes, respectively.



From the picture, one can see that:

- The leading edges of the pulses are equally spaced.
- All the pulse trains are DC balanced.
- The first pulse is either wide or narrow for self-framing. This provides the indication of the start point of the frame after a long normal clock train.
- The disparity of a pulse cancels the disparity of the earlier pulse.

The encoder and decoder for the C5 scheme have been tested in an Altera Cyclone FPGA. An oscilloscope screen dump is shown in the following picture.



The traces in channel 1 are C5 pulse trains that the first pulse is either wide or narrow. The pulse trains are used to drive both sequential logics and a phase-lock-loop (PLL) circuit in the FPGA. The recovered clocks from the PLL are shown in Channel 3 and 4. The messages are extracted and a data valid signal is fed into channel 2. The data valid pulse seen on screen comes from the previous 5-pulse train outside the left edge of the screen. We trigger on the data valid pulse from the 5-pulse train in the screen. Note the position of the trigger marker.